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The DG535/536 Wideband Multiplexers Suit a Wide Variety of Applications

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Introduction

Analog switch IC's traditionally have found limited use in applications involving high-frequency analog or digital signals. Degradation of switch performance and intolerable signal cross-talk between channels has undoubtedly forced many designers to use bulky electromechanical switches or costly discrete designs.

At best, analog switch ICs configured in L or T arrangement could be adopted. However, increased board space and layout complexity became major problems in configuring systems with high channel density.

The DG535/536 are compact 16-channel, single-ended multiplexer ICs, primarily designed as a cost-effective solution to video and wideband switching problems. Other applications that benefit from the devices' superior performance characteristics are:

- Digital switching
- Audio Switching
- PCM routing networks
- ATE systems
- High-channel-density multiplexing or demultiplexing systems
- High-speed multiplexing systems
- Low-level signal multiplexing

Product Description

A functional block diagram of the DG535/536 is shown in Figure 1 and the switch configuration is shown in Figure 2. The device is fabricated using self-isolated, silicon-gate D/CMOS technology. This process enables the logic interface and driver circuitry, the gating and latching stages, and the switching elements to be combined in a monolithic structure.

Ease of design for large switching matrices and interface with microprocessors is accomplished with comprehensive logic gating and latching functions available on the chip.
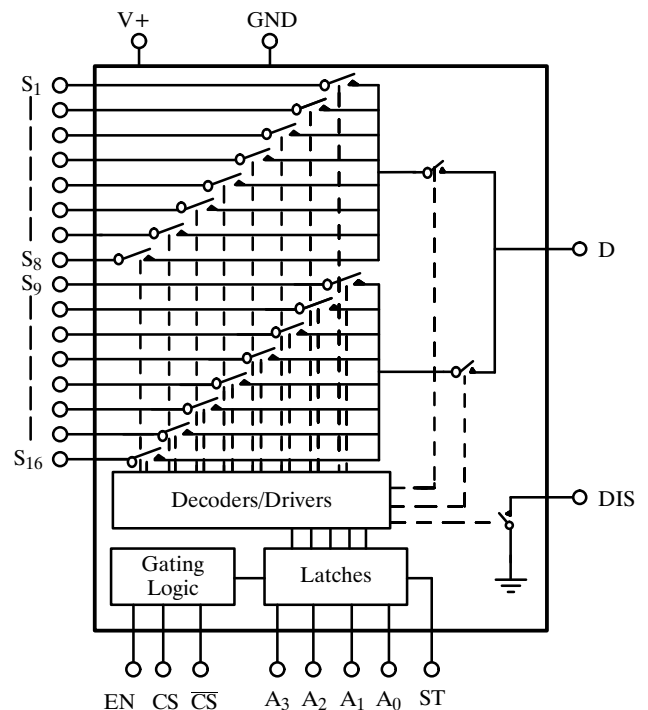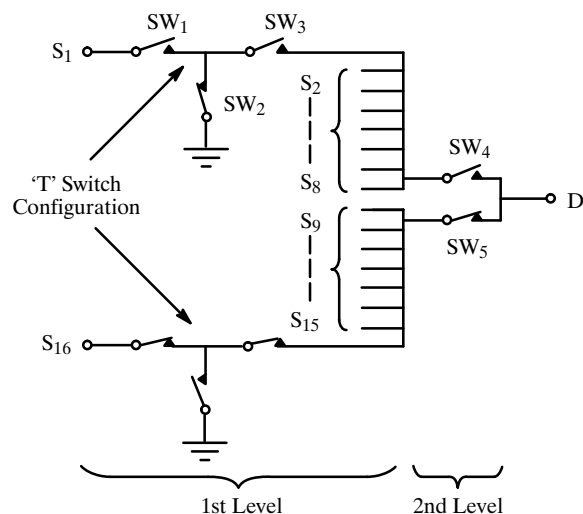

Figure 1. DG535/536 Functional Block Diagram
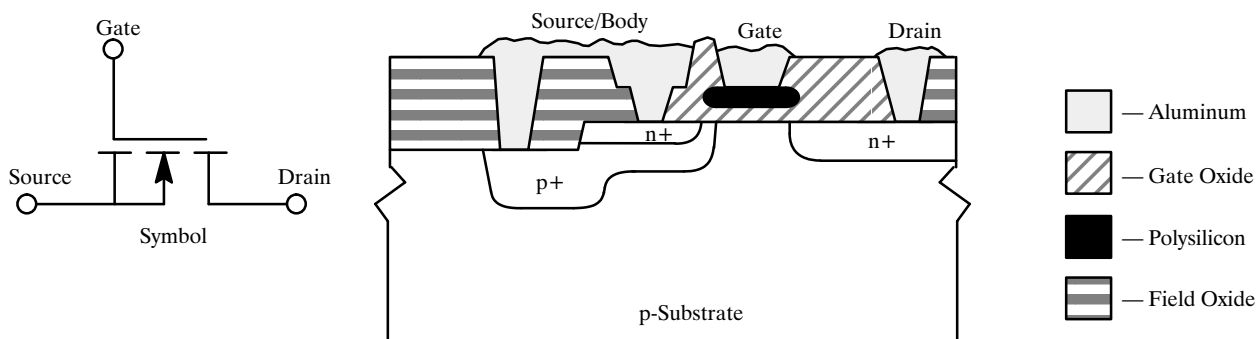

Figure 2. Switch Configuration

The DG536 is housed in a small, 44-pin J-lead package, thus minimizing board size requirements. The DG535 is packaged in a 28-pin DIP. Chip select pins (CS and $\overline{CS}$) permit easy stacking of devices for multi-channel multiplexing systems (see Applications Section, Figure 19).

An additional feature, a DIS pin, is an open drain terminal with the source tied to the device substrate. The DIS terminal represents a high impedance to the substrate (normally ground) when the DG535/536 is disabled and a low impedance to ground when the DG535/536 is enabled. This output can be used to indicate which device in a large matrix has been enabled (see Figure 13), or it can be used to switch off circuitry following the multiplexer stages.

Minimizing Parasitic Effects

The insertion loss and bandwidth of the switch are improved with DMOS transistors that offer a low on-resistance and low intrinsic capacitance (see Siliconix SD5000 data sheets). on the DG536 channel-to-channel crosstalk is minimized by physically separating each input channel with a GND pin which extends to the device substrate. This, in conjunction with careful PC board layout (see Figure 6), can yield channel-to-channel crosstalk figures better than -92 dB at 5 MHz.

Further ac performance benefits are obtained through the n-channel DMOS transistor T configurations (Figure 2). This maximizes the off-isolation, since SW_2 provides a shunt path to ground for any signals fed through the parasitic capacitance associated with SW_1. SW_3 (working in phase with SW_1) provides an extra stage of off-isolation and prevents the shunt switch (SW_2) from affecting consecutive channels.

Two-Level Switching

The two-level switching system of the DG535/536 (SW_4 and SW_5) works out of phase, effectively isolating half of the switch outputs from the drain (output) of the multiplexer. These series switches serve several functions:

- They provide an extra stage of off-isolation.

- They reduce the drain output capacitance significantly and increase the multiplexing transition speed.

- They reduce the off-leakage current, which reduces the offset voltage that develops from the total off-leakage current flowing through the load resistance and/or switch on-resistance. This enables lower analog signal levels to be handled accurately.

Silicon Gate

Polysilicon is used as the transistor gate material for the DG535/536, as opposed to more conventional metal-gate designs. This technology minimizes the charge coupling of the control-logic signals to the switch output due to the self-aligning properties of the process. Metal-gate technology relies on photolithographically aligning the gate metal with the channel diffusions, resulting in greater overlap tolerances.

As shown in Figure 3, a PN junction exists between the p-type substrate and the n-type channel diffusions. This junction should not become forward biased by the analog signal going more negative than the substrate potential (normally ground).

Figure 3.   Cross-Section of an N-Channel, Silicon-Gate DMOS Transistor

Device damage could result from the current flow through the forward biased substrate-channel junction, exceeding the aluminum current handling capacity (i.e. 20 mA). Analog signal dc biasing or offsetting the device power supplies can prevent this problem. These methods are discussed in the applications section of this paper (Figure 7 and Figure 8).

DG535/536 DC Characteristics

On-Resistance

On-resistance must be low to ensure low insertion loss, especially when the switch drives low load resistances. As shown in Figure 4, the on-resistance remains low and fairly constant over the usable analog signal range. This makes the DG535/536 useful for audio applications that require low harmonic distortion.
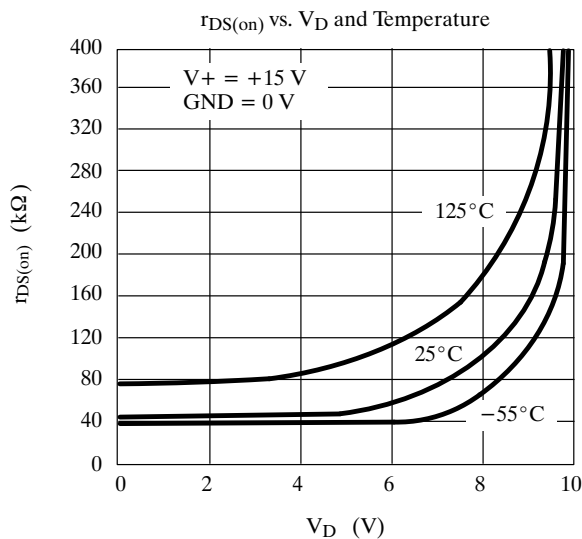
$r_{DS(on)}$ vs. V_D and Temperature

Figure 4. On-Resistance vs. Analog Signal Characteristics

Nominal $r_{DS(on)} = 50\ \Omega$

Insertion Loss $= 20\ LOG_{10}\ \dfrac{V_{OUT}}{V_{IN}}$

Figure 5. 600 Ω Audio System
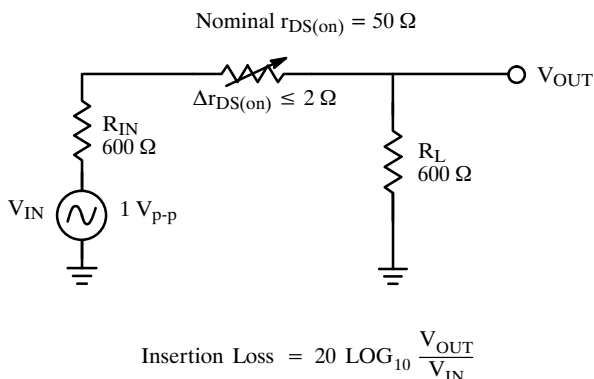
In a 600-Ω audio system, such as the one represented in Figure 5, the percentage of on-resistance change relative to the load resistance is only 0.33%. The insertion loss due to the switch on-resistance is 0.7dB.

Leakage Current

The DG535/536 features low off and on leakage currents, reducing switching errors.

Power Supply Current Consumption

Until now, most available video multiplexers or digital crosspoint switches relied on high-level supply currents for operation. The DG535/536 requires a total supply current of only 5 μA, typical. This feature makes the DG535/536 ideal for systems with high channel density, such as 32-channel crosspoint matrices used in video mixing consoles or as ECL digital crosspoint replacements in large data transmission systems.

The total supply current for a 32-channel crosspoint system using the DG535/536 is approximately 320 μA, much lower than other video multiplexers.

DG536 AC Characteristics

(Refer to the DG535 data sheet for the 28-pin DIP performance.)

Bandwidth

The "on" frequency response is expressed as the frequency at which the insertion loss (at dc) increases by 3 dB. The measured bandwidth of the DG536 is greater than 300 MHz.

Crosstalk

Crosstalk is the amount of unwanted signal apparent at a particular node due to the parasitic capacitance of the device. As the most important parameter for many applications, crosstalk is specified in a number of ways.

1. **Single-channel crosstalk** is the ratio of the signal seen at the drain (output) to the signal applied to a single off-channel input. This is expressed by

$$XTALK_{(SC)}(dB)\ =\ 20\ log_{10}\ \frac{V_{OUT}}{V_{IN}}$$

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Most conventional multiplexers specify this parameter on the data sheet as off-isolation. This value for the DG536 is more than twice as good as other 16-channel analog multiplexer ICs, proving the effectiveness of the T switch.

2. **All hostile crosstalk** is the ratio of the signal measured at the drain to the signal applied simultaneously to all 15 channels (i.e., with one channel on).

3. **Chip-disabled crosstalk** is the drain output to signal input ratio. The input signal is applied to all 16 off channels simultaneously.

4. **Adjacent input crosstalk** is the ratio of the signal applied to a source (input) to the signal measured at any adjacent source. A low adjacent input crosstalk is required for video applications to avoid ghosting effects that may appear on video monitors or TV screens.

Switching Time

The DG535/536 switching time enables use of the device at high multiplexing rates. The low transition times (t_{ON} = 300 ns maximum and t_{OFF} = 150 ns maximum) make it ideal for fast multi-channel analog or digital multiplexing.

True break-before-make (BBM) switching action is guaranteed by design. This prevents shorting (crosstalk) of time adjacent input channels during transition.

Capacitance

Capacitance determines the loading effect of the multiplexer on signal sources and affects transition times, as well as system bandwidth.

1. **Off-state input capacitance** gives the loading of the device (in the off-state) to a signal source. With a typical value of 2 pF, this allows efficient paralleling of many device channels in multi-channel crosspoint matrices with negligible loading effects.

2. **On-state input capacitance** also determines the loading effects of the device on-signal sources and limits the number of parallel on channels allowed in a large matrix. In large matrixes buffering of the input signals is recommended.

3. **Off-state output capacitance** affects the transition speed of the multiplexer. The output capacitance must be charged and discharged in turning on and off a device; thus, a low value of capacitance enables rapid transition times. Table 1 shows a comparison of DG536 capacitance to comparable 16-channel multiplexers.
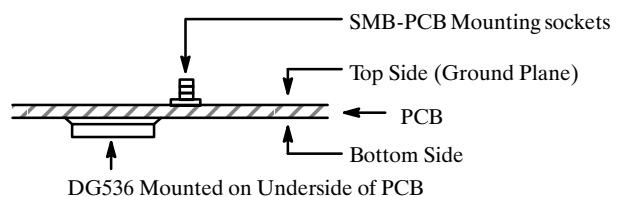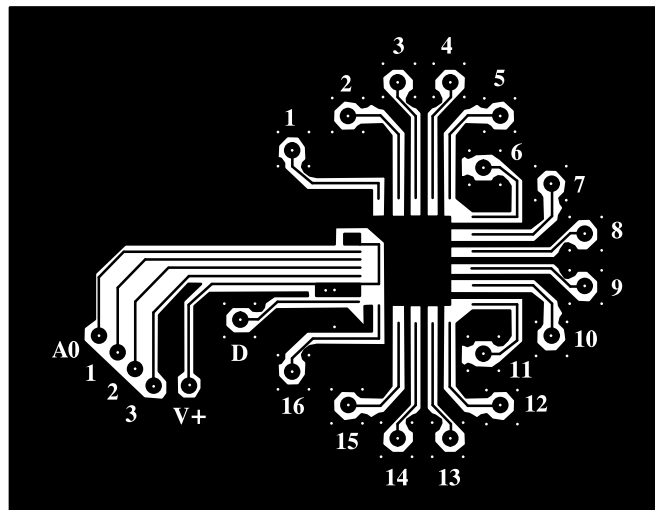
Circuit Board Layout

To optimize the high-frequency characteristics of the DG536, care must be taken in circuit board layout and interconnections. Parasitic stray capacitances caused by poor layout could degrade performance significantly. As shown in Figure 6, use of guard planes and traces between signal paths is a good layout practice. Other layout considerations include:

- Short signal paths
- Sufficient power supply decoupling
- Coaxial interconnect of leads, plugs, and sockets.
- Sockets should be avoided

Applications

Many applications for the DG535/536 will be in video related systems. Some examples of circuit configurations are included in this section.

Figure 6. Circuit Board Layout for Optimal Performance (DG536)

Table 1. Capacitance Value for 16-Channel Multiplexers

Parameter	DG526	DG506A	DG508A	CD4051/2/3	DG536
$CS_{(off)}$ (pF)	10	6	5	10	2
$CD_{(off)}$ (pF)	65	46	26	60	8

Note: These are typical values taken from data sheets

Video

The DG536 was designed primarily for handling broadcast quality video signals. Optimum performance is achieved with a bias between $+2.5$ V and $+3$ V. Differential phase linearity is best at this bias level.

A general-purpose 16-channel wideband multiplexer is shown in Figure 7. Dc biasing is achieved with the divider network R_1 and R_2. A wideband op-amp (Si582) is configured to give an inverting unity gain, while removing the $+3$ V dc by setting the voltage on the non-inverting input to $+1.5$ V dc. The use of trimpot R_7 and precision resistors allows accurate elimination of any dc bias. This arrangement results in faster multiplexing rates than capacitive decoupling while providing black-level clamping, impedance matching for 75 Ω loads, and greater drive for

transmission stages, with no major compromise on signal quality (distortion, frequency response, etc.)

Alternatively, the device supplies can be offset to eliminate the need for 16 separate bias circuits. Such an arrangement, shown in Figure 8, could be used in a security system or in a remote industrial monitoring system. The DG535/536 positive supply and ground pins (at -3 V) should be heavily decoupled to the video camera ground connections.

The switching threshold of the device at a supply voltage of $+15$ V is approximately between $+6$ V and $+8.5$ V above the substrate potential (Figure 9). Since the substrate is held at -3 V, the effective switching threshold referenced to ground is between $+3$ V and $+5.5$ V. Thus, the device can still be controlled from CMOS logic signals (provided that the logic 0 (V_{AL}) is less than 3 V and logic 1 (V_{AH}) is greater than $+5.5$ V).
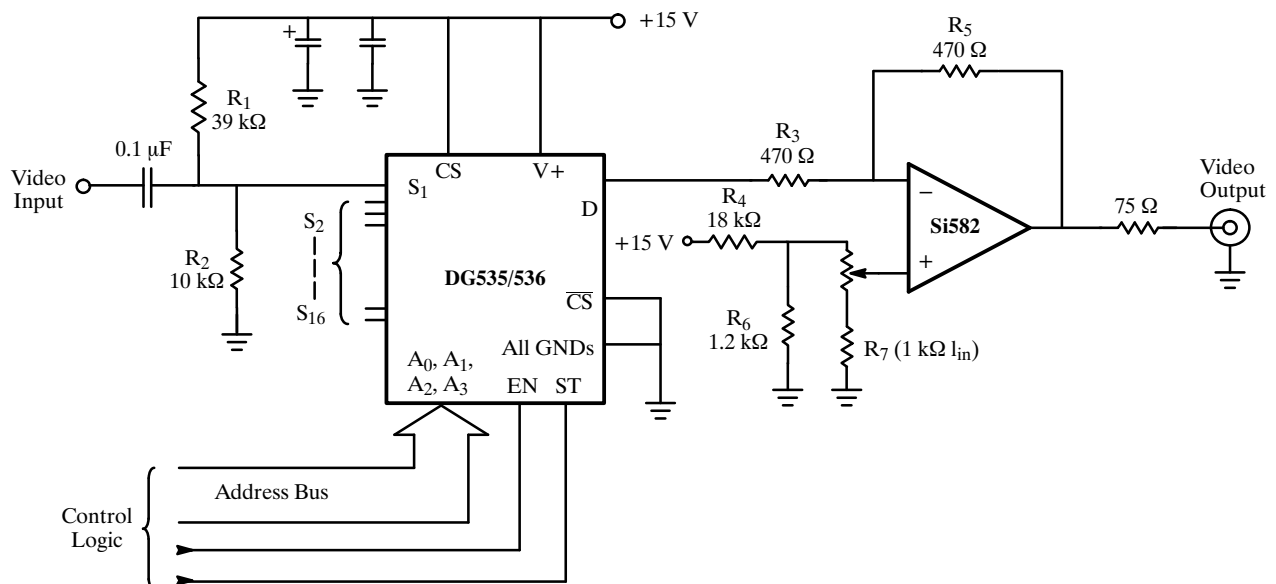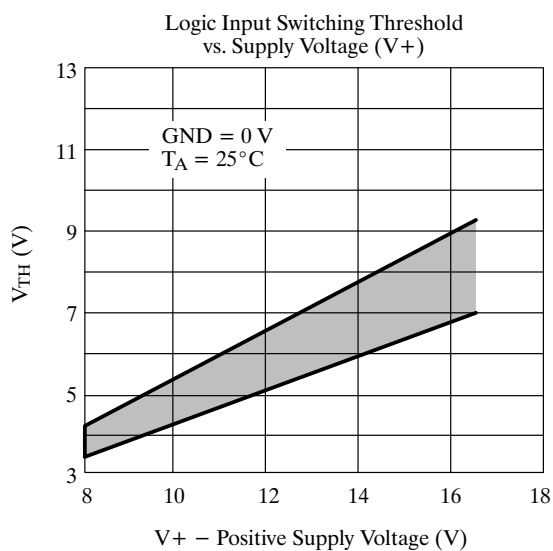

Figure 7. General-Purpose 16-Channel Wideband Multiplexer
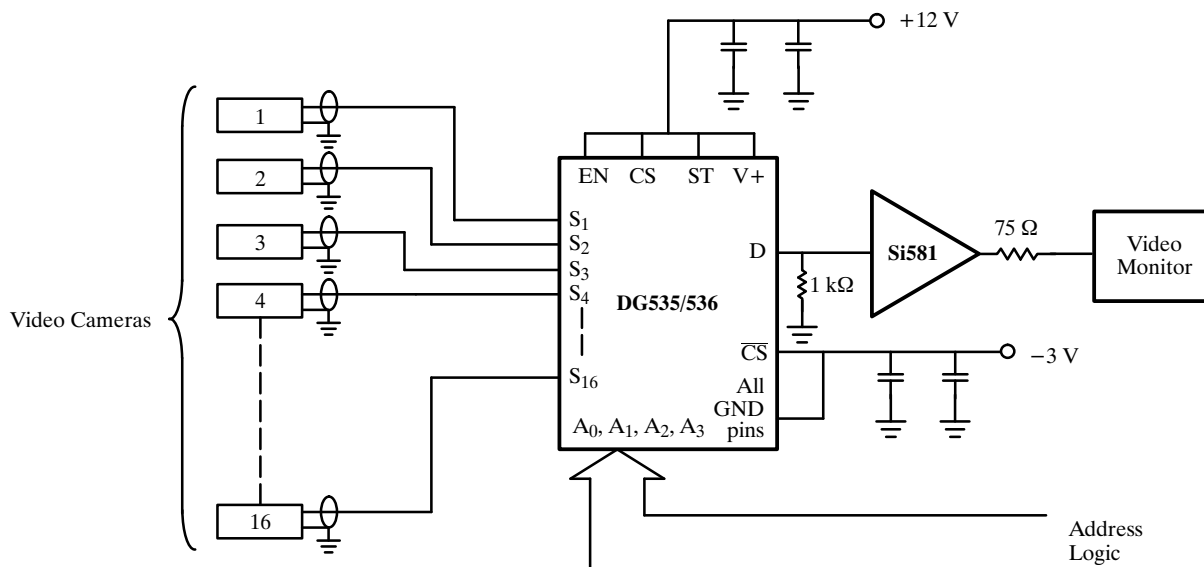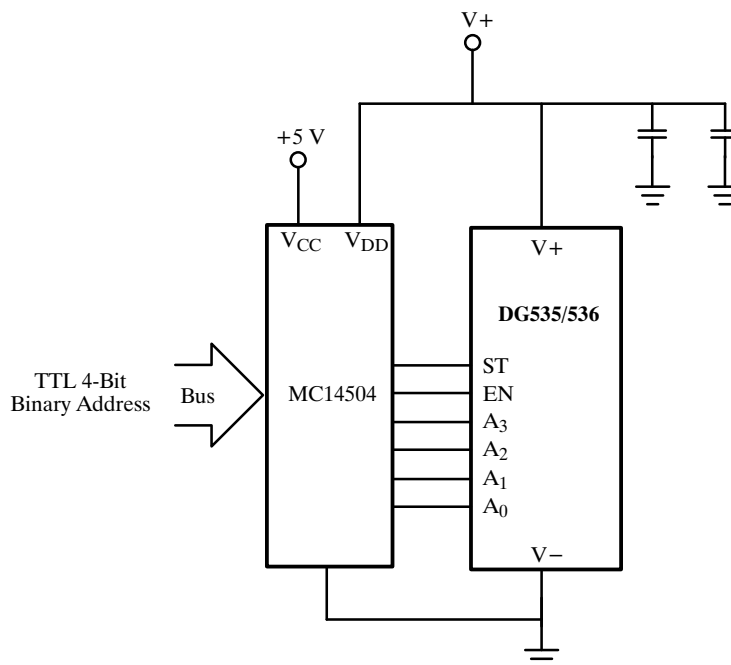
Figure 8. A Closed-Circuit Monitoring System

Figure 9. Logic Input Switching Threshold
vs. Supply Voltage

Figure 10. Using the MC14504 for Address Logic
Level Shifting

In applications involving reduced supply voltages and offset conditions, the input switching threshold (V_T) may be reduced below the CMOS logic "0". This may cause the address inputs to appear permanently as logic "1" regardless of the control logic states. Therefore, control logic level shifting may be needed.

TTL to CMOS level shifting can be easily accomplished using inexpensive CMOS level shifters such as the MC14504 or CD40109.

Crosspoint Switching

Many analog and digital systems, such as a central router used in a video studio console (Figure 8), require crosspoint switching functions. In this application, many channels route signals to many different outputs. Due to its small outline PLCC package and low power consumption, the DG536 leads itself easily to multi-channel crosspoint functions.

Figure 11 illustrates how the DIS (disable) pin can be used to indicate which output is selected. When logic 1 is applied to output select, device 1 is enabled and device 2 is disabled. With device 1 enabled, the DIS pin is connected to signal ground, thus turning LED 1 on. With device 2 disabled (due to $\overline{CS}$ being 1), its DIS pin represents a high impedance to ground and LED 2 is off.

Any one of sixteen inputs can be connected to either output. This is achieved by applying the appropriate CMOS logic address to the address inputs (A_0 to A_3) and applying the appropriate logic level to output select simultaneously.

The circuit in Figure 11 also illustrates how the chip select inputs can be used. As shown in Figure 12, a 32-channel single-ended multiplexer can be configured without external chip select circuits. This circuit makes use of the CS and $\overline{CS}$ inputs which allow device selection from a single control line.

The basic circuit shown in Figure 11 can be extended and elaborated to give a 16 x 16 matrix for video crosspoint applications such as central routers used in video studios. This circuit, shown in Figure 13, allows source (or video input) to be connected to any video output (or any number of outputs). The strobe input (ST) on each device is used to latch the appropriate address into that particular device. By strobing the required address into each device sequentially, any crosspoint connection can be made.
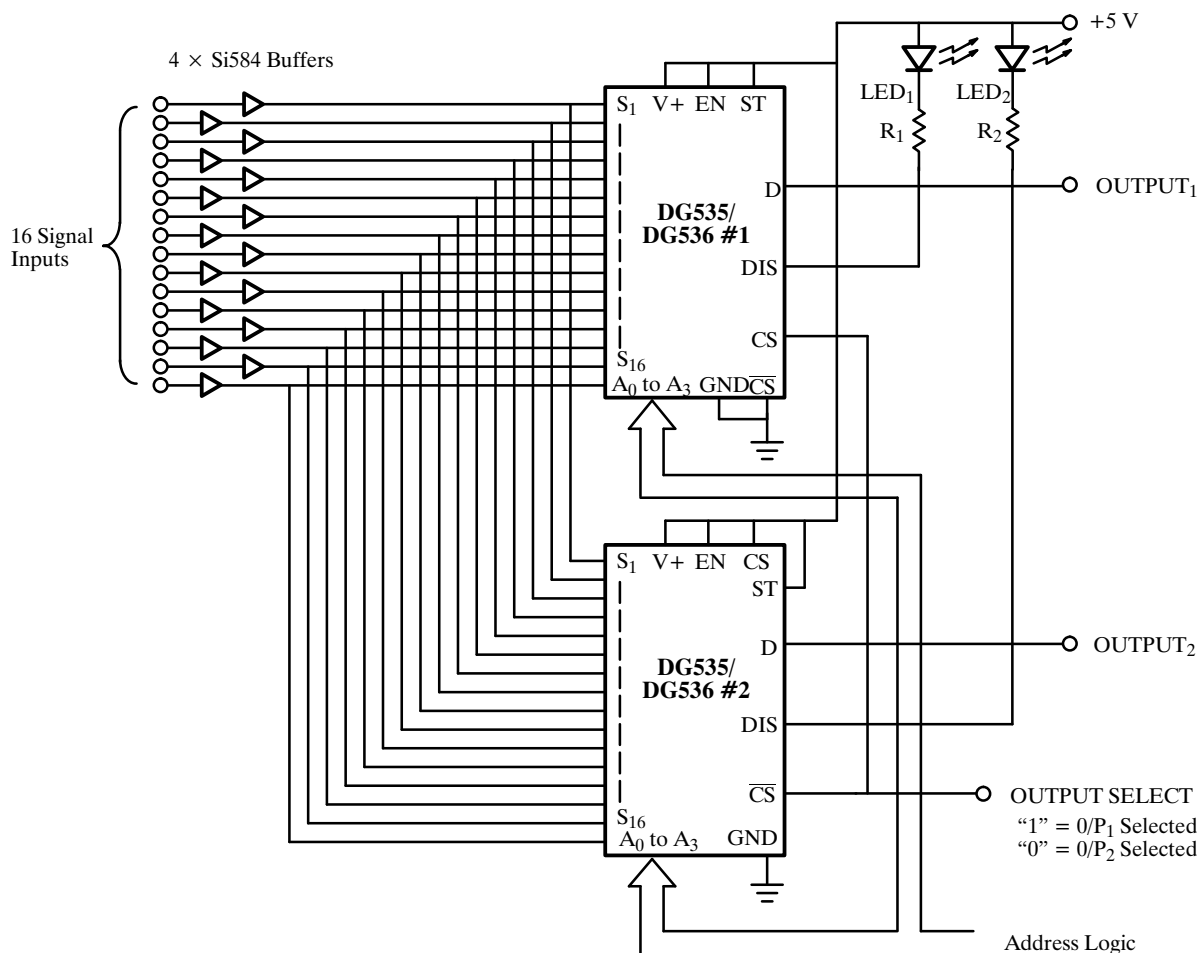

Figure 11. The DG535/536 as a 16 × 2 Matrix Switch
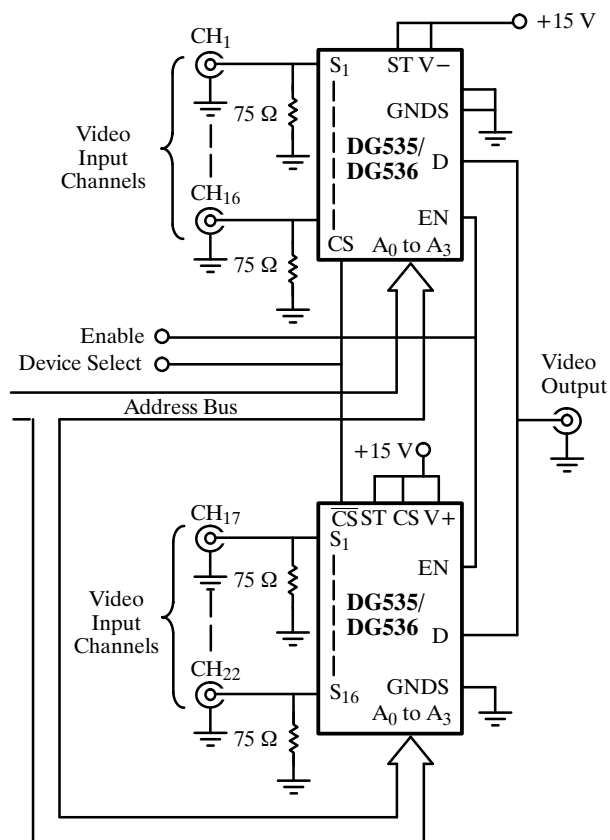
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Figure 12. 32-Channel Multiplexer

The DG535/536 makes an excellent digital switch due to its low channel-to-channel crosstalk, high off-isolation, and wide bandwidth specifications. In digital data transmission systems, the DG535/536 can easily handle data rates in excess of 100 Mb/s.

The circuit shown in Figure 13 can be used as a digital cross-point to replace expensive, power consuming ECL crosspoint ICs. Besides handling raw digital data, the DG535/536 can also be used for other forms of data transmission, such as FSK and PCM systems.

FSK

Frequency shift keying (FSK), commonly used in data transmission networks, relies on representing the digital code with frequency sine wave bursts. An FSK multiplexing system block diagram is shown in Figure 14. Each digital level has a specific signal frequency. The DG535/536 can be used to multiplex 16 different digital channels into a single transmission line or into a transmitter. Similarly, a DG535/536 may be used to demultiplex the data at the

receiving end. Since the device can manipulate higher frequency sine waves, data can be transmitted at a higher rate than with a conventional multiplexer.

PCM

A more commonly used and faster form of digital data transmission is known as PCM (pulse coded modulation). Used in telecommunications systems, PCM converts analog speech signals into 8-bit digital words for serial transmission. The data transfer rate used (for 4 kHz bandwidth voice signals) is up to 274.176 Mbps.

The DG535/536 can be used to route PCM signals in main telephone exchanges, replacing bulky hard-wired distribution frames. PCM highways can thus be rerouted remotely, under computer control, rather than manually.

RZ (returns to zero) PCM data consists of three discrete (ternary) levels to overcome long periods of zeroes (Figure 13). Digital signals can degrade beyond legibility after only a few hundred yards of travel down a transmission line. Therefore, the PCM signals must be regenerated at regular distances to avoid excessive distortion.

Figure 16 shows the architecture of a conventional binary distribution frame in a telephone exchange. Signal regeneration is applied to handle degradation during
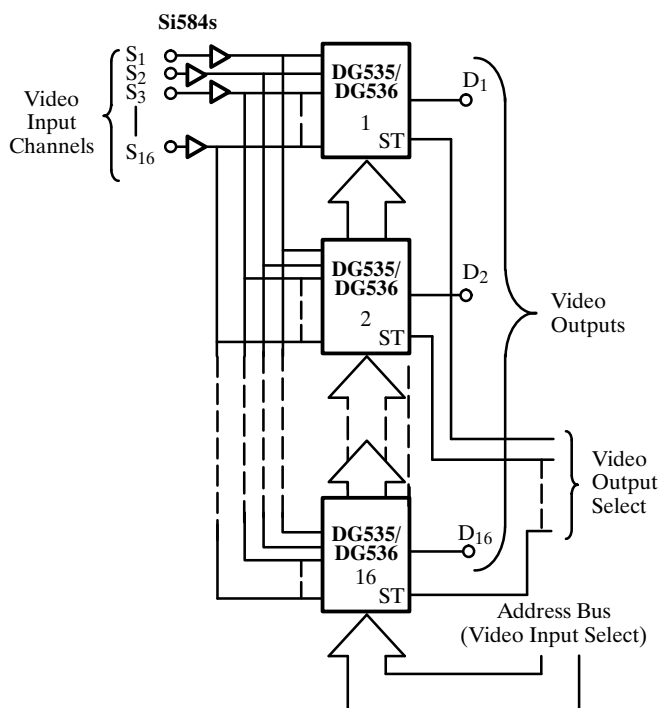

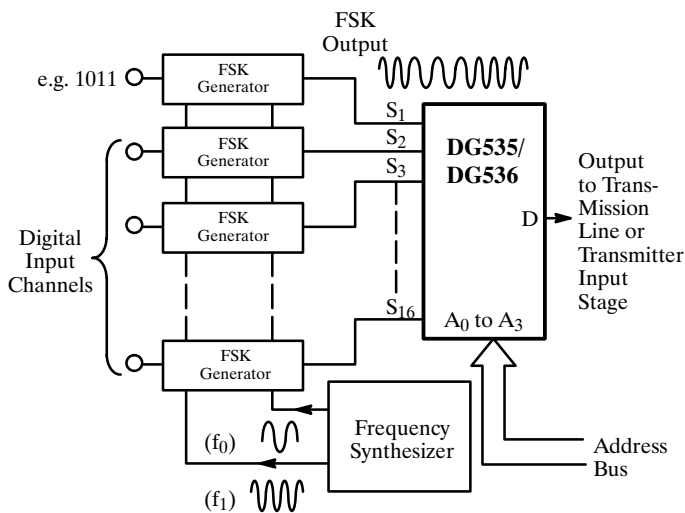**Figure 13.** 16 x 16 Video Crosspoint Circuit

Figure 14. FSK Multiplexing System Block Diagram

a) Analog voice signal converted to digital signal using 8 bits per sample

b) Digital signal transmitted and clock regenerated from digital signal to get synchronization
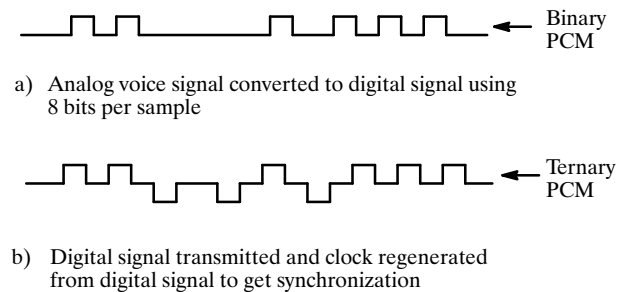
Figure 15.

transmission and routing. Code converters are required to change the ternary PCM into binary PCM for routing within the distribution frame. Similarly, code converters are required to reconvert the binary PCM into ternary PCM for transmission.

Unlike digital switches which require specific digital signals, using the DG535/536 in the distribution frame (Figure 17) eliminates the need for code conversion and meticulous regeneration because it can handle analog signals.
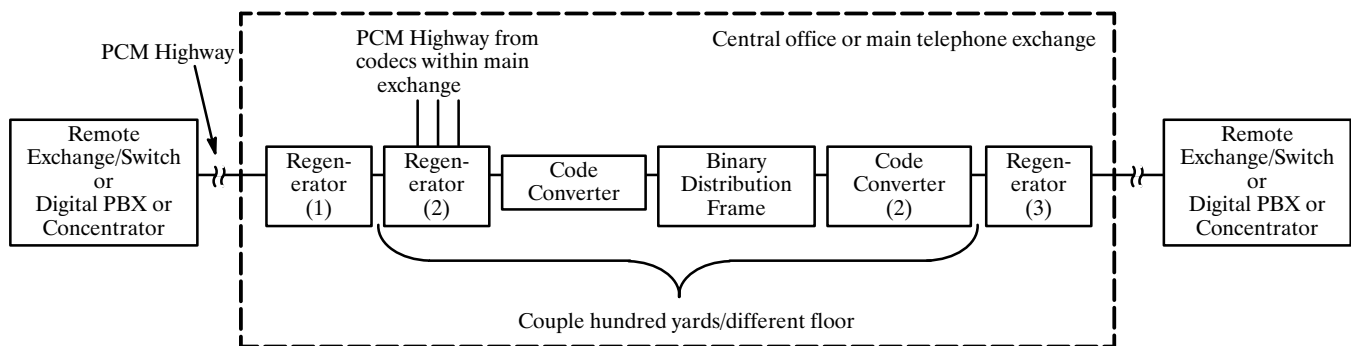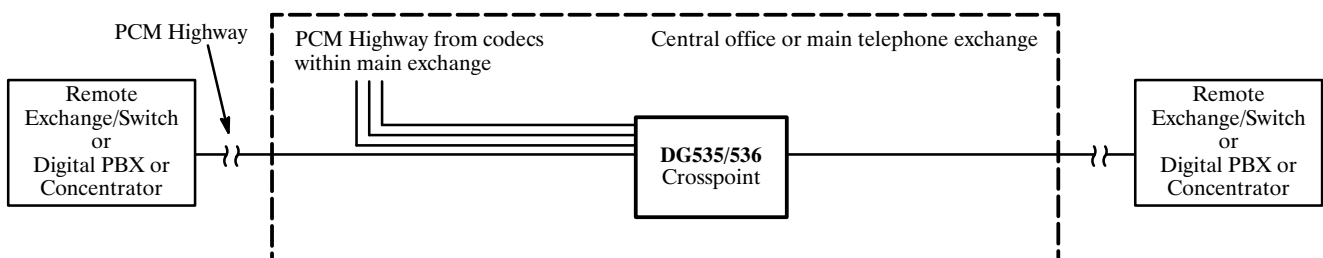

Figure 16. Binary PCM Routing Network

Figure 17. DG536 PCM Distribution Frame

Programmable Gain Video Amplifier

The circuit shown in Figure 18 uses the DG536 as a binary gain select for a video/wideband op-amp (Si582).

The gain of the Si582 is set by:

$$A_V = 1 + \frac{R_f}{R_g}$$

For example, listed below in Table 2 are the results when $R_f = 470\ \Omega$.

Table 2. Gains for the Circuit of Figure 18.

Logic Input	R_g	Gain (A_V)
0000	47 kΩ	1.0
0001	4.7 kΩ	1.1
0010	2.4 kΩ	1.2
0011	1.6 kΩ	1.3

The low on-resistance of the DG535/536 gives good gain stability, and the resistor tolerances mainly determine the gain error of the circuit.

The wideband qualities of the Si582 allows this circuit to be employed for digital level correction in any video systems including broadest quality specifications.
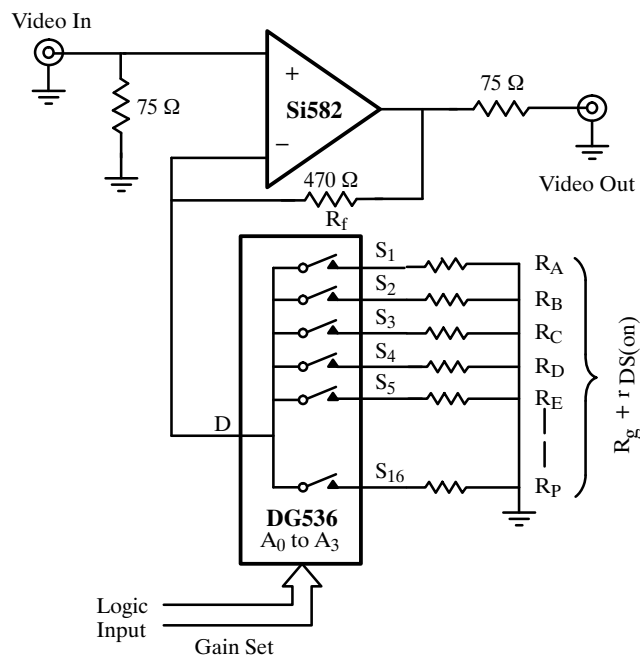
Figure 18. Programmable Gain Video Amplifier

ATE

A simple but accurate ATE system, as shown in Figure 19, can be designed for testing digital processing boards.

The propagation delay time for each of the 16 digital signal paths can be tested individually, with negligible errors due to the very small propagation delay through the DG535/536. Also, the variation of delay times from channel to channel is less than 0.25 ns.

Microprocessor Interface

On-chip data latches in the DG535/536 simplify interface with a microprocessor data bus. This eliminates the need for peripheral memory devices (such as I/O ports or D-type latch ICs) to maintain switch addressing while the processor uses its data bus for other functions.

The data latches are activated by the DG535/536 strobe input (ST). The latch is transparent when ST= logic 1, thus the device responds to changes of data at the address inputs. When ST = logic 0, the previous data is latched into the device, regardless of new data appearing at the address inputs.

The DG535/536 timing arrangements meet the requirements of popular microprocessors, such as the 8085A, 6800, and Z80. The 8085A to DG535/536 interface is shown in Figure 20, and Table 3 illustrates the timing compatibility of the DG535/536 with the 8085A and the faster 8085A-2 devices.
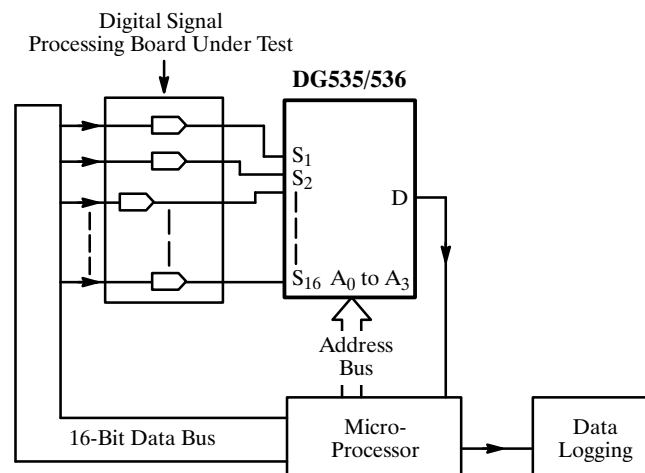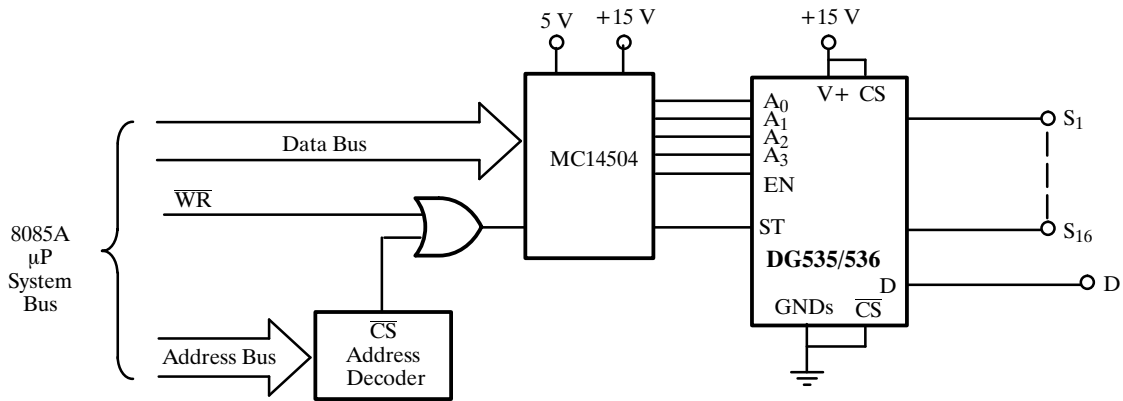

Figure 19. ATE Applications

Figure 20. 8085A to DG535/536 Interface

Figure 21 shows the complete 6800 to DG536 interface circuit. In order to have a data valid signal, it is necessary

Table 3. Timing of the DG538/536 with Popular Microprocessors

Specification	8085A ns/min.	8085A-2 ns/min.	DG536 ns/min.
t_{SW} (strobe pulse width)	400	230	200
t_{DW} (data valid to strobe)	420	230	100
t_{WD} (data valid after strobe)	100	60	50

to nand the R $/\overline{W}/\overline{CS}$ gate output with the Φ_2 clock (usually connected to the DBE pin). This makes the interface circuit functionally compatible with the 8085A interface shown in Figure 20.

Note that open collector gates and buffers could be used to level shift the TTL logic levels from the microprocessor to the CMOS levels required by the DG535/536 logic inputs.

To achieve the correct ST signal in a Z80 processor system, the $\overline{WR}$ and $\overline{MREQ}$ signals must be gated with the standard $\overline{CS}$ signal, as shown in Figure 22.
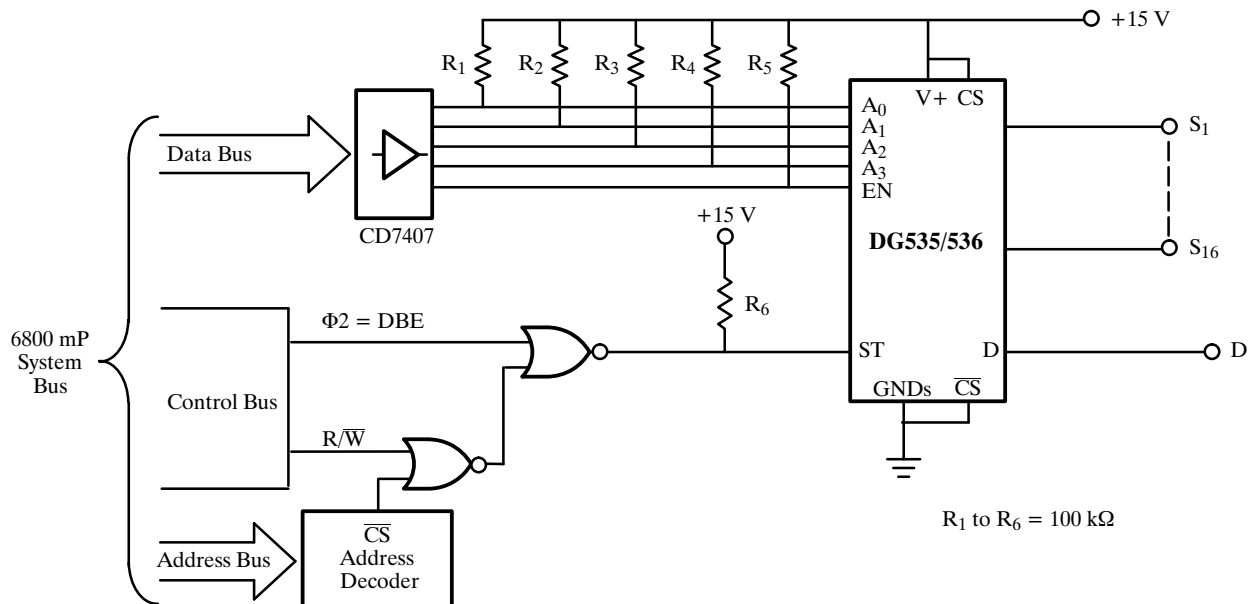

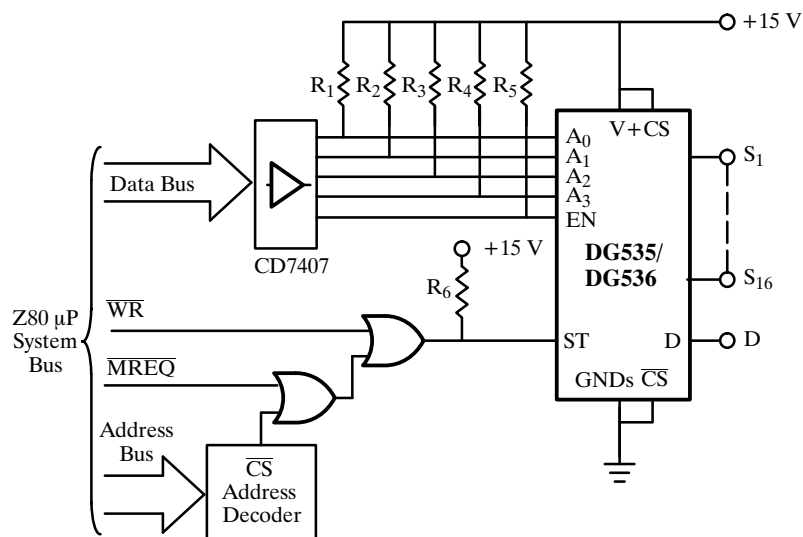**Figure 21.** 6800 to DG535/536 Interface
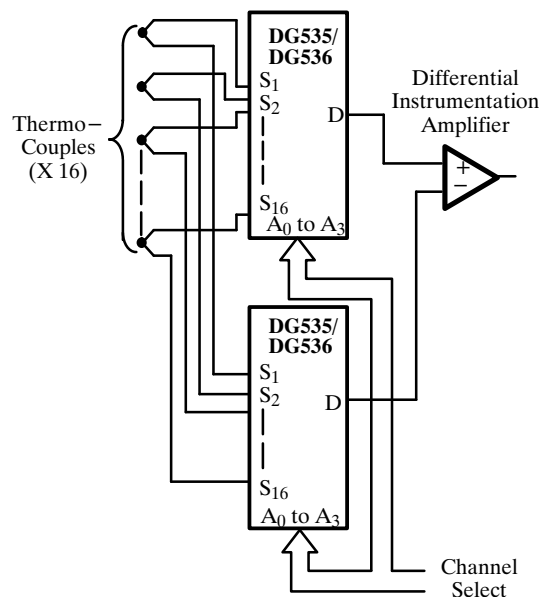
Figure 22. Z80 to DG536 Interface

Figure 23. Thermocouple Multiplexing System

Low Analog Signal Switching/Multiplexing

The DG535/536 has several uses in handling low-level analog signals (such as in medical equipment or ultrasound transducer multiplexing) because the device exhibits inherently low noise and offset voltages. Two factors affect offset voltage:

1. Thermoelectric offset voltage is produced by the incidental thermocouples that exist within the integrated circuit. There are many intermetallic junctions within an IC. These junctions act as an individual thermocouple and has an identical reversed counterpart. That is, from source to drain, we have gold-aluminum/aluminum-silicon and silicon-aluminum/aluminum-gold. Therefore, if the temperature surrounding each junction is constant and equal, the thermal EMFs cancel each other, giving a zero net offset voltage. Since a thermal gradient always exists across the chip, then there is always a net thermoelectric offset voltage. For the DG535/536, the thermal EMFs produced on chip are small since the device exhibits a low power consumption (75 μW), producing a low temperature on the die.

2. Leakage current offset is caused by leakage current flowing through the r_{DS} of an on-switch and/or the

load resistance. The offset voltage developed due to leakage current is negligible since the device has very low leakage currents (a benefit incurred by the two-level system) coupled with very low on-resistance.

For example:

$$V \text{ (offset)} = I_{D(on)} \text{ x } r_{DS(on)}$$
$$= \pm 100 \text{ pA (typical @ } 25^\circ\text{C)} \times 55 \text{ } \Omega \text{ (typical)}$$
$$= \pm 5.5 \text{ nV (typically)}$$

The circuit shown in Figure 23 can be used to remotely monitor up to 16 different thermocouples with high accuracy. The output of the thermocouples is in the form of a small dc voltage, on the order of millivolts, with typical voltage changes on the order of tens of microvolts per $^\circ$C. Thus, voltage offset developed by the switching devices can frequently limit system accuracy.

Using the differential multiplexing technique shown in Figure 23, high resolution can be achieved since the thermal EMFs produced by each DG535/536 are canceled as common mode voltages at the instrumentation amplifier inputs. To minimize pick-up and noise effects, the same PC board layout rules apply for this type of circuit. Best accuracy is achieved by ensuring that the multiplexers are kept close together in a thermally stable environment.